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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/082,472 | 02/22/2002 | Akito Yoshida | W2K 1077 | 4326 |

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| EXAMINER | |
|---|---|
| ZARNEKE, DAVID A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 10/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/082,472 | YOSHIDA, AKITO | |
| | Examin r | Art Unit | |
| | David A. Zarneke | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *8/8/03* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments, see page 14, section I, filed 8/8/03, with respect to Otake have been fully considered and are persuasive. The nonfinal rejection over Otake of 5/6/03 has been withdrawn.

Applicant's arguments with respect to Fujisawa have been fully considered but they are not persuasive.

Regarding the Fujisawa rejection, it is argues that Fujisawa can only be used for lead devices and not the other types of devices claimed.

The examiner asserts that the rejection of the claims using Fujisawa are directed to the claims that either broadly read upon lead types or explicitly claim lead type devices. The claims directed to other types of devices, namely 7 and 8, are not rejected using Fujisawa.

With respect to the Fujisawa rejection, it is further argued that Fujisawa fails to teach a flexible substrate for stacking.

The examiner asserts that Fujisawa does indeed teach a flexible substrate for stacking. As seen in Figures 5A-5C, the lead (24) is bent around the packaged chip and then multiple packages can be stacked (figures 9 A & B, 10 A & B, 11, 12 A & B, and 13-23). Therefore, if the lead can be bent, it must be flexible.

Applicant's arguments filed with respect to Chung have been fully considered but they are not persuasive.

First, it is argued that Chung uses a flexible interposer without metal layers for stacking.

The examiner asserts that Chung (figure 20) does indeed teach metal layers (413) within the interposer having dielectric layers (411-1 to 411-3).

Lastly, it is argued that Chung uses vias and solder balls to stack the packages.

The examiner takes the position that the present claims do not exclude the use of vias and solder balls. The claims only assert that the substrate is used for stacking. Chung teaches connecting the metal layers (413) of adjacent packages using solder balls, which the present claims do not excluded.

The previous rejections that are being maintained will now be re-stated.

***Claim Rejections - 35 USC § 102***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 4, 5, 9, 11, 21, 24 and 25 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Fujisawa et al., US Patent 5,801 ,439.

Fujisawa teaches a semiconductor structure comprising:

a first semiconductor device (21); and

a flexible substrate means (24) coupled to a bottom surface of the first semiconductor device, wherein the flexible substrate is folded over on at least two sides to form flap portions which are coupled to an upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device (Figures 4, 5A-C).

Regarding claims 4 and 24, Fujisawa teaches the stacking of a 2nd device coupled to the flap portions of the substrate (Figures 9A, 9B, 10A & 10B).

With respect to claims 5 and 25 the stacking of a 2nd device coupled to the flap portions of the substrate after the flaps have been folded over onto the 1st device (Figures 9A, 9B, 1OA & 10B).

As to claim 9, Fujisawa teaches a lead-type device (Figures and abstract).

***Claim Rejections - 35 USC § 102***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 2, 4, 5, 8, 11, 12, 21, 22, 24, 25 and 28 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chung, US Patent 6,376,769.

Chung teaches a semiconductor stacking structure comprising:

a first semiconductor device (420); and

a flexible substrate means (410) coupled to a bottom surface of the first semiconductor device, wherein the flexible substrate is folded over on at least two sides to form flap portions which are coupled to an upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device (Figures 19 & 20).

Regarding claims 2, 12 and 22, Chung teaches placing adhesive 41 1-3 on the interposer that attaches the interposer to the device (Figure 19 & 21, 54+).

With respect to claims 4 and 24, Chung teaches coupling a 2Dd device to the folded flap of the 1st device (Figure 21).

As to claims 5 and 25 Chung teaches attaching the 2/d device after the flaps have been folded over and coupled to the 1St device.

Regarding claims 8 and 28, Chung teaches the stacked structure to be a BGA device (30, 19+).

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 3, 7, 23 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung, US Patent 6,376,769.

Regarding claims 3 and 23, Chung fails to teach the use of an adhesive layer which is placed on the upper surface of the first semiconductor device and which couples the flap portions to the first semiconductor device.

The placement of an adhesive on the chip instead of on the interposer or in addition to being on the interposer is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the ad (MPEP 2144.04(d)).

With respect to claims 7 and 27, Chung fails to teach the specific use of this invention in a LGA, but does teach that it may be used in combination with other conventional surface mounting technology (30, 19+).

Therefore, since LGA is a conventional surface mounting technology, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the invention of Chung in a LGA device.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claims 6 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung, US Patent 6,376,769, as applied to claims 1, 11 and 21 above, and further in view of Iwase, US Patent 6,172,418, or Hashimoto et al., US Patent 6,486,544, or Kim et al., 6,225,688, or Nicewarner, Jr. et a1., US Patent 5,776,797.

Chung fails to teach the 2nd device coupled to the flap portions of the flexible substrate before the flap portions are folded over and coupled to the 1st device.

Iwase, Hashimoto, Kim and Nicewarner all teach a stacked chip package wherein chips are placed on a flexible insulating film before folding into a stacked package.

It would have been obvious to one of ordinary skill in the ad at the time of the invention to use the device attached to the flaps before folding of Iwase, Hashimoto, Kim and Nicewarner in the invention of Chung because these references teach that it is conventionally known in the art to formed stacked packages in this manner.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chung, US Patent 6,376,769, as applied to claims 1, 11 and 21 above, and further in view of Fujisawa et al., US Patent 5,801 ,439.

Chung fails to teach the semiconductor stacking structure as being a lead type device.

Fujisawa teaches a package wherein a chip is molded in an encapsulant with leads extending out of and bent around the outside the package (Figures 4 & 5A-C).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the lead-type package of Fujisawa in the invention of Chung because Chung teaches that the invention may be used in combination with other conventional surface mounting technology (30, 19+) and a lead-type package is a conventional surface mounting technology.

The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chung, US Patent 6.376.769, as applied to claims 1, 11 and 21 above, and further in view of Otake et al., US Patent 5,805,422.

Chung fails to teach flexible substrate is folded over on four sides to form flap portions, which are coupled to the upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device.

Otake teaches a flexible circuit board having four sides that are folded over onto the attached chip (Figures 7-9 & 11).

It would have been obvious to one of ordinary skill in the ad at the time of the invention to use the four-sided folds of Otake in the invention of Chung because Otake teaches that fewer fabricating steps are required (7, 55+), bending of the chip is minimized and failures of the pads at the time of installation is eliminated (7, 62+).

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to David A. Zarneke at (703)-305-3926. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703)-308-1233. The fax phone number where this application is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703)-308-6789.

David A. Zarneke
October 3, 2003 AU 2827